In re Appln. of Furumoto et al.
Serial No. Unassigned

IN THE ABSTRACT

Please replace the existing Abstract of the Disclosure with the appended Abstract of the Disclosure.

REMARKS

The foregoing changes are made to improve the form of the patent application. No new matter has been added and entry is respectfully requested.

A favorable Action on the merits is solicited.

Respectfully submitted,

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ABSTRACT OF THE DISCLOSURE

In a method of designing a semiconductor circuit having clock trees, a netlist is first generated. Then, delay dates are inserted into the netlist. Finally, inserted extra delay gates are deleted so that a timing constraint of the clock trees is satisfied. As a consequence, skew between the clock trees can be easily adjusted.